Assignee: Intel Corporation

IN THE CLAIMS

Presented below is a complete listing of the claims.

Claims 1 through 19 (cancelled)

20. (New) An apparatus, comprising:
a first register file of a plurality of register files to store predicate values; and
a second register file of said plurality of register files to receive results from execution of a first instruction that writes to multiple predicate registers when said first register file is busy.

21. (New) The apparatus of claim 20, further comprising a select register to indicate which of said plurality of register files is being written to by execution of a second instruction that writes to multiple predicate registers.

22. (New) The apparatus of claim 21, wherein said select register includes a pointer to said which of said plurality of register files.

23. (New) The apparatus of claim 20, wherein said first register file indicates that is it busy with a scoreboard.

24. (New) The apparatus of claim 23, wherein said apparatus stalls execution of a third instruction that writes to at most two predicate registers when said scoreboard indicates destination registers of said third instruction are busy.

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25. (New) The apparatus of claim 20, further comprising a free file list to point to the next in order of said plurality of register files that is not busy.

26. (New) The apparatus of claim 25, wherein said free file list indicates which of said plurality of register files are to be de-allocated.

27. (New) A method, comprising:

storing predicate values in a first register file of a plurality of register files; and

allocating a second register file to receive results from execution of a first instruction that writes to multiple predicate registers when said first register file is busy.

28. (New) The method of claim 27, further comprising indicating which of said plurality of register files is being written to by execution of a second instruction that writes to multiple predicate registers.

29. (New) The method of claim 28, wherein said indicating includes using a select register to point to said which of said plurality of register files.

30. (New) The method of claim 27, further comprising indicating busy status with a scoreboard.

31. (New) The method of claim 30, further comprising stalling execution of a third instruction that writes to at most two predicate registers when said scoreboard indicates destination registers of said third instruction are busy.

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32. (New) The method of claim 27, further comprising pointing to a next in order one of said plurality of register files that is not busy.

33. (New) The method of claim 32, further comprising de-allocating one of said plurality of register files when said pointing indicates a earlier in order one of said plurality of register files is not busy.

34. (New) A system, comprising:

a processor including a first register file of a plurality of register files to store predicate values, and a second register file of said plurality of register files to receive results from execution of a first instruction that writes to multiple predicate registers when said first register file is busy;

an interface logic to couple said processor to input/output devices; and

a disk drive logic coupled to said processor via said interface logic.

35. (New) The system of claim 34, wherein said processor includes a select register to indicate which of said plurality of register files is being written to by execution of a second instruction that writes to multiple predicate registers.

36. (New) The system of claim 34, wherein said first register file indicates that is it busy with a scoreboard.

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37. (New) The system of claim 36, wherein said processor stalls execution of a third instruction that writes to at most two predicate registers when said scoreboard indicates destination registers of said third instruction are busy.

38. (New) The system of claim 34, wherein said processor includes a free file list to point to the next in order of said plurality of register files that is not busy.